Arjun Prakash

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Education

Nanyang Technological University 2024 – 2028
Bachelor of Engineering in Electrical and Electronics Engineering Singapore
Second Major in Data Analytics GPA: 4.01/5.00

Experience

Panasonic R&D Singapore Jun 2026 – Present
Physical AI & ML Research Intern *Singapore*

- Deployed and evaluated VLA and imitation-learning policies, including π0.5, GR00T N1, ACT and Diffusion Policy, with work spanning UR5/UR5e, Unitree G1 and RoboParty V1 platforms.
- Built RGB-D geometry, camera-calibration and trajectory-auditing tools for manipulation experiments, using ROS 2 and MoveIt 2 Servo for policy and control integration.
- Designed and trained PPO policies in Isaac Lab, engineering rewards and trajectory- and position-seeded training workflows; developed motion-retargeting workflows for robot-learning experiments.
- Built Docker-orchestrated Isaac Sim/Isaac Lab workflows with a ROS 2 control path shared between simulation and hardware; cross-validated Isaac PhysX and MuJoCo models against real torque measurements.
- Developing geometry-conditioned ACT for in-hand reorientation using CAD-free RGB-D geometry and gripper state; manuscript in preparation for IROS 2027 with NTU MARS Lab.

Nanyang Technological University Jul 2026 – Present
Undergraduate Researcher – 3D Perception & World Models *Singapore*

- Implemented voxelized LiDAR initialization for Gaussian semantic occupancy, with optional density-based opacity priors and an unchanged 28-D interface to the downstream encoder and decoder.
- Built a mask-aware occupancy evaluator with strict checkpoint loading, per-class IoU, GPU latency and peak-memory reporting to support controlled camera–LiDAR comparisons.
- Designing confidence-gated temporal Gaussian updates to reuse reliable geometry and prioritize uncertain or changed regions, aiming to reduce recomputation latency while preserving occupancy accuracy; targeting ICCV 2027.

Nanyang Technological University Jul 2025 – Jun 2026
Undergraduate Researcher – Computer Vision & Edge AI *Singapore*

- Trained a ResNet18 PCB-defect classifier to 85.3% accuracy and adapted an SSD300 ADAS detector to 44.6% mAP@0.5 across four safety-critical classes; presented at IEEE ICIEA 2026.
- Built a custom Verilog convolution accelerator on Xilinx ZCU104, achieving 3.3× faster inference and 6.3× lower energy per image than the onboard ARM CPU.
- Applied INT8 post-training quantization with under 0.4 percentage-point accuracy loss; recalibrated confidence thresholds to recover 93% defect recall without retraining.

Projects

Text-Guided RGB-D Object Localization

- Built text-guided RGB-D localization using segmentation, depth filtering and calibrated transforms; achieved approximately 85–95% object-finding success and 5–15 mm position error, with queries taking a few hundred milliseconds.

Robot Demonstration Quality Inspector

- Built a robot-demonstration auditor linking video and action traces; detected nearly 100% of frozen frames and timestamp gaps, and approximately 70–90% of jerky or idle segments.

Task-Aware Joint-Space Safety Envelope Implemented

- Built a task-specific runtime guardrail from recorded joint angles and speeds that rejects out-of-envelope commands, aborts execution and returns explicit diagnostics.

Leadership

MLDA@EEE – Main Committee, Business Development Aug 2025 – Present
Managed NVIDIA, Micron and industry partnerships; led teams delivering applied-ML projects and technical showcases.

Technical Skills

Robot Learning: Behavior cloning, ACT, Diffusion Policy, PPO, VLA policy integration (π0.5, GR00T N1)
3D Perception: RGB-D/LiDAR, Gaussian occupancy, point-cloud registration (ICP), DINOv2 features, camera calibration
Robotics and Simulation: ROS 2, MoveIt 2 Servo, Isaac Sim, Isaac Lab, MuJoCo, simulation/hardware validation
ML and Inference: PyTorch, ONNX export, INT8 post-training quantization, latency/memory benchmarking
Programming and Systems: Python, C/C++, Docker, Linux, Git

Publication

A. Prakash and X. S. Loo, "FPGA-Accelerated Edge Vision: PCB Defect Detection and ADAS Object Detection on Xilinx ZCU104," IEEE ICIEA 2026, Catania, Italy. Presented.